**You have to submit this report via Moodle.**

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| Design of Digital Circuits: Lab Report | | |
| Lab 1: Drawing Basic Circuits | | |
| Date |  | Grade |
| Names |  |  |
|  |  | Lab session / lab room |
|  |  |  |

**Use a zip file or tarball that contains the report and other required material. Only one of the members of each group should submit. All members of the group will get the same grade.**

**The name of the submitted file should be *Lab1\_LastName1\_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.**

**Exercise 1**

**(a)** Assume that we were only using 2-input AND gates and 2-input XNOR gates to create our comparator in Part 1 in this week’s lab manual. How many of each gate would you use for a comparator of width 8, 16, 32 and 64 bits? What is the logic depth in each case?

*Note: the logic depth of a combinational circuit is defined as the number of logic gates in the longest signal path (path from input to output).*

|  |  |  |  |
| --- | --- | --- | --- |
| Comparator Width | 2-input XNOR gates | 2-input AND gates | Logic depth |
| 8 bits |  |  |  |
| 16 bits |  |  |  |
| 32 bits |  |  |  |
| 64 bits |  |  |  |

**(b)** Given the comparator width is N, derive general expressions for calculating the following:

(i) The number of 2-input XNOR gates

(ii) The number of 2-input AND gates

(iii) The logic depth

**Exercise 2**

Use two instances of the 1-bit comparator we designed in Part 2 in this week’s lab to implement a 2-bit comparator. Draw the schematic of your design.

**Exercise 3**

What is the logic depth of each of the output ports in the circuit of Exercise 2?

**Feedback**

If you have any comments about the exercise please add them here: mistakes in the text, difficulty level of the exercise, anything that will help us improve it for the next time.